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In the Claims

1.   (Original) An integrated circuit, comprising:

an antifuse including a first terminal, a second terminal and a gate dielectric between the first terminal and the second terminal, the first terminal being connected to a line;

a program driver circuit coupled to the second terminal of the antifuse; and

a bypass circuit coupled to the line and the program driver circuit, the bypass circuit being adapted to shunt current around the antifuse during a programming mode.

2.   (Currently Amended) The integrated circuit of claim 1, wherein the bypass circuit includes a plurality of diodes.

3.   (Original) The integrated circuit of claim 2, wherein the plurality of diodes includes a plurality of transistors coupled together as series-connected diodes.

4.   (Original) The integrated circuit of claim 3, wherein the plurality of transistors include p-channel transistors.

5.   (Original) The integrated circuit of claim 1, wherein the gate dielectric includes at least one of an oxide and an oxynitride.

6.   (Original) An integrated circuit, comprising:

a line to provide a programming voltage during a programming mode and to provide a common voltage during a non-programming mode;

an antifuse including a first terminal connected to the line, a second terminal and a gate dielectric between the first terminal and the second terminal;

a program driver circuit coupled to the second terminal of the antifuse; and

a bypass circuit coupled to the line and the program driver circuit in parallel with the antifuse, the bypass circuit being adapted to shunt current around the antifuse during the programming mode with the antifuse not being selected to be blown.